REMARKS

Drawings

Claim Rejections - 35 U.S.C. §§ 102/103

The Examiner has rejected claims 1, 8, 9, and 12 under 35 U.S.C. § 102(b) as being anticipated by Krivokapic '587. The Examiner has rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9, and 12 above, and further in view of Takeuchi '351. The Examiner has rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 as applied to claim 1, 8, 9, and 12 above, and further in view of Choi '582. The Examiner has rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 in view of Takeuchi '351 as applied to claim 2 above, and further in view of Choi '582. The Examiner has rejected claims 5 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9, and 12 above, and further in view of Choi et al. '088. The Examiner has rejected claim 14 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 in view of Pfiester '315 in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi '582.

With respect to claims 1-14, Applicant teaches and claims a semiconductor device comprising a gate electrode formed on a gate dielectric, wherein the gate electrode has a lower portion formed directly on the gate dielectric layer. The semiconductor device includes a pair of inwardly concaved source/drain regions on opposite sides of the gate electrode which create "***inflection points b neath said lower portion of said gate electrode formed directly on said gate di l ctric***

layer". That is, Applicant's teach and claim that the inflection points lie beneath the gate dielectric layer upon which the lower portion of the gate electrode is directly formed.

Applicant does not understand Krivokapic as describing a device which includes inflection points formed beneath the lower portion of the gate electrode which is formed directly on the gate dielectric layer. Applicant understands Krivokapic to describe a device having source/drain regions 217 and 218 and a gate electrode 210 which is formed on a gate dielectric layer 208. In Krivokapic, the furthest the source and drain regions extend are beneath the sidewalls spacer 219. In Krivokapic, the source and drain regions do not extend beneath the lower portion of the gate electrode 210 which is formed directly on the gate oxide layer 208 (See Figure 2o).

Additionally, as stated in previous responses, the source and drain regions of Krivokapic extend at their furthest point beneath the sidewall spacers 219. The sidewall spacers 219 are formed on sacrificial oxide layer 202 and not gate dielectric layer 208 (See Figure 2G). The gate oxide layer 208 is subsequently formed between the sidewall spacers as shown in Figure 2g. Krivokapic specifically states that the upper surface of the gate oxide layer 208 extends between the boundaries of the spacers 219 and the gate structure cavity 240 to replace the gate pad oxide 202 that was previously removed. As such, the source and drain regions 217 and 218 in Krivokapic, extend underneath the remaining sacrificial oxide layer 202 and not beneath the gate oxide layer 208.

As such, for the above mentioned reasons, it is Applicant's understanding that Krivokapic fails to teach or render obvious source and drain regions having inflection points which extend beneath the lower portion of the gate electrode which is formed directly on the gate dielectric layer as claimed by Applicant. Applicant,

therefore, respectfully requests the removal of 35 U.S.C. § 103 rejections of claims 1-14 based upon Krivokapic.

With respect to claims 3, 4, and 14, Applicant teaches and claims a device wherein the gate dielectric layer is thicker beneath the outside edge of the gate electrode than the gate dielectric layer beneath the center of the gate electrode. It is the Examiner's position that on one of ordinary skill in the art would combine Krivokapic with Choi and Takeuchi to obtain Applicant's invention as claimed in claims 3, 4, and 14. It is Applicant's understanding that one of ordinary skill in the art would not combine Krivokapic with Choi because the processes and structures described in the cited references are incompatible with one another. Krivokapic describes a process which utilizes a replacement gate technique to form the gate electrode. In the replacement gate technique, a gate structure cavity 240 (Figure 2d) is formed and a gate electrode 210 and spacer 219 formed therein. The goal of the process taught by Krivokapic is the formation of a transistor gate electrode without the use of photolithography to pattern the gate electrode (Col. 3, lines 11-14). Additionally, the process results in a gate electrode structure which is wider at the top than at the bottom (T-shaped). Choi, on the other hand, forms a gate electrode 23 which is wider at the bottom than at the top (inverse T-gate)(See Figure 3c) in order to allow the edges to bend upward to form a thicker gate oxide layer at the edges of the gate electrode during the subsequent oxidation (Figure 3d). Additionally, the gate structure in Choi is formed utilizing a photolithography process (Figure 3a) to form the electrode which is precisely what Takeuchi wishes to avoid. Thus, in order to form a thicker gate oxide layer at the edges, Choi forms a gate electrode having an opposite shape than Krivokapic and which uses a process (photolithography patterning) which Krivokapic wishes to avoid. As such, the teachings of Choi are direct conflict with Krivokapic. The Examiner has provided no teaching or suggestions whatsoever on how one of ordinary skill in the art would

combine these two opposite gate electrode structures and formation techniques. As such, one of ordinary skill in the art would not combine Choi with Krivokapic. For the above mentioned reasons, it is Applicant's understanding that the combination of Krivokapic and Choi fail to teach or render obvious Applicant's invention as claimed in claims 3, 4, and 14 for this reason also.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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